Al-Mansoura University | Logic Circuits 2
Faculty of Engineering | 2nd year Students
Communications and Elect. Dept | January 2013 | Time 3 Hours

Attempt in all questions and assume any missing data.

Q1-(a)- Draw the following logic circuits, explain its operations, and write its truth table: (1)-Active-Low S-R latch, (2)-Gated S-R latch, (3)- Positive edge triggered D flip flop, (4)-Negative edge triggered J-K flip flop with asynchronous reset and clear inputs.

(b)- For a gated S-R latch, determine the Q and $\overline{Q}$ outputs for the inputs in Figure (1). Show them in proper relation to the enable input. Assume that Q starts LOW.

(10 marks)

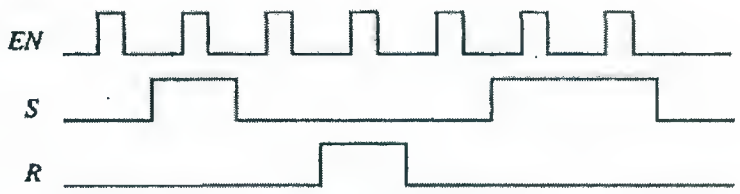

Figure (1)

Q2- (a)- Define the following terms: (1)-Propagation delay times, (2)-Set-up time, (3)- Hold time, (4)-Maximum Clock Frequency, and (5)-Pulse Widths.

(b)- Determine the Q waveform relative to the clock if the signals shown in Figure (2) are applied to the inputs of the J-K flip-flop. Assume that Q is initially High.

(10 marks)

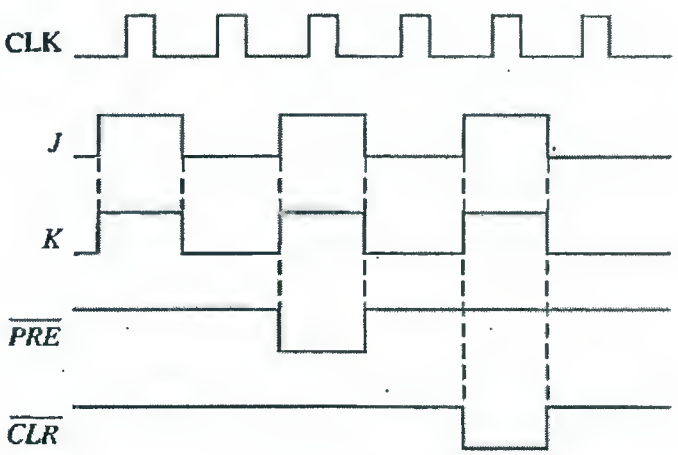

Figure (2)

Q3-(a)-Design with drawing the timing diagram of the following counters: (1)- 3-bit asynchronous binary counter, (2)- Synchronous BCD counter, (3)- 3-bit up/down synchronous binary counter.

(b)-Show the timing diagram and determine the sequence of a 4-bit synchronous binary up/down counter if the clock and UP/DOWN control inputs have waveforms as shown in Figure (3). The counter starts in the all 0s state and is positive edge-triggered. (20 marks)

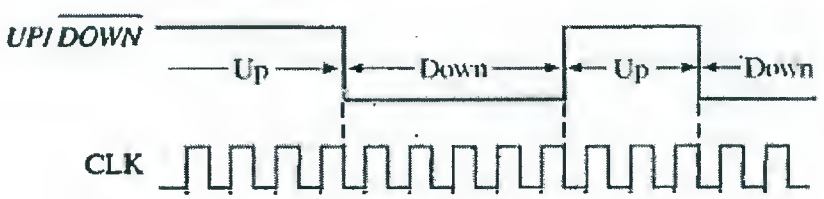

Figure (3)

Q4- (a)-Design a 4-bit parallel in/serial out shift register and describe its operation.
(b)-The shift register in Figure (4-a) has SHIFT/$\overline{\text{LOAD}}$ and CLK inputs as shown in Figure (4-b). The serial data input (SER) is a 0. The parallel data inputs are $D_0 = 1$, $D_1 = 0$. $D_2 = 1$, and $D_3 = 0$ as shown. Develop the data-output waveform in relation to the inputs. (10 marks)

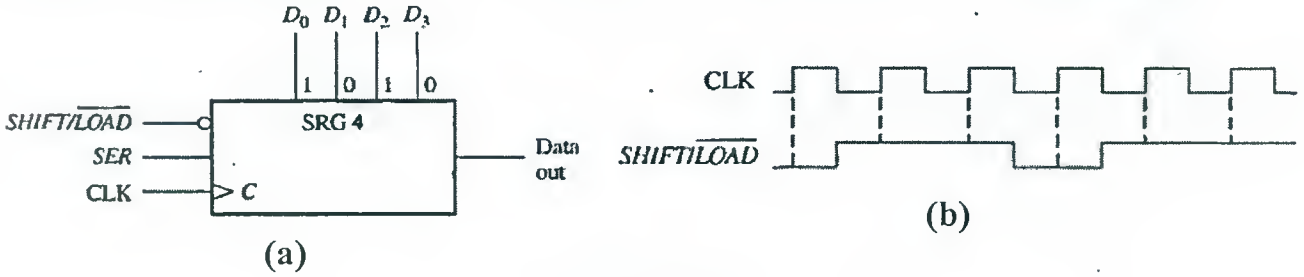

Figure (4)

Q5- (a)-Design a 4-bit bidirectional shift register and describe its operation.
(b)- Determine the state of the bidirectional shift register of part (a) after each clock pulse for the given RIGHT/LEFT control input waveform in Figure (5). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$. and $Q_3 = 1$ and that the serial data-input line is LOW.

(10 marks).

Figure (5)

Q6:(a)- Draw the block diagram of a 3-dimensional RAM memory showing address bus, address decoders, bidirectional data bus, and read/write inputs. Explain the function of each component.
(b)-Design an SRAM memory with the following specifications:
(1)-Memory capacity is 128 rows x 256 columns x 8 bit.
(2)-The control signal lines are $\overline{\text{CS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$.
(3)-Bidirectional data buses are used. (10 marks)

Q7:(a)-Explain with drawing the following basic operation of the DRAM:
(1)-Writing a 1 into the memory cell. (2)- Writing a 0 to memory cell.
(3)-Reading a 1 from the memory cell.

(b)-Explain with drawing the following basic operation of the flash memory cell: (1)-The programming of 0 and 1 in a flash cell,
(2)-The read operation of 0 and 1. (10 marks)